(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
19 February 2004 (19.02.2004)

PCT

(10) International Publication Number
WO 2004/016036 A2

(51) International Patent Classification[7]: H04R

(21) International Application Number: PCT/US2003/024777

(22) International Filing Date: 8 August 2003 (08.08.2003)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
60/402,220 8 August 2002 (08.08.2002) US
10/638,057 7 August 2003 (07.08.2003) US

(71) Applicant *(for all designated States except US)*: **THE BOARD OF TRUSTEES OF THE LELAND STANFORD JUNIOR UNIVERSITY** [US/US]; 1705 El Camino Real, Palo Alto, CA 94306-1106 (US).

(72) Inventors; and
(75) Inventors/Applicants *(for US only)*: **KHURI-YAKUB, Butrus, T.** [US/US]; c/o Stanford University, 1705 Camino Real, Palo Alto, CA 94306-1106 (US). **HUANG, Yongli** [—/US]; c/o Stanford University, 1705 El Camino Real, Palo Alto, CA 94306-1106 (US). **ERGUN, Arif, S.** [TR/US]; c/o Stanford University, 1705 El Camino Real, Palo Alto, CA 94306-1106 (US).

(74) Agents: **TEST, Aldo, J.** et al.; Dorsey & Whitney LLP, 4 Embarcadero Center, Suite 3400, San Francisco, CA 94111 (US).

(81) Designated States *(national)*: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, YU, ZA, ZM, ZW.

(84) Designated States *(regional)*: ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IT, LU, MC, NL, PT, RO, SE, SI, SK, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:
— *without international search report and to be republished upon receipt of that report*

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(54) Title: MICROMACHINED ULTRASONIC TRANSDUCERS AND METHOD OF FABRICATION

(57) Abstract: There is described a micromachined ultrasonic transducers (MUTS) and a method of fabrication. The membranes of the transducers are fusion bonded to cavities to form cells. The membranes are formed on a wafer of sacrificial material. This permits handling for fusions bonding. The sacrificial material is then removed to leave the membrane. Membranes of silicon, silicon nitride, etc. can be formed on the sacrificial material. Also described are cMUTs, pMUTs and mMUTs.

WO 2004/016036 A2

MICROMACHINED ULTRASONIC TRANSDUCERS AND METHOD OF FABRICATION

RELATED APPLICATION

This application claims priority to U.S. Provisional Application Serial No. 60/402,220 filed August 8, 2002.

BRIEF DESCRIPTION OF THE INVENTION

This invention relates generally to micromachined ultrasonic transducers (MUT) and more particularly to a method of fabricating micromachined ultrasonic transducers using wafer-bond technology and to the resultant MUTs.

BACKGROUND OF THE INVENTION

Ultrasonic transducers have been used in a number of sensing applications such as a medical imaging non-destructive evaluation, gas metering and a number of ultrasound generating applications such medical therapy, industrial cleaning, etc. One class of such transducers is the electrostatic transducer. Electrostatic transducers have long been used for receiving and generating acoustic waves. Large area electrostatic transducer arrays have been used for acoustic imaging. The electrostatic transducer employs resilient membranes with very little inertia forming one plate of an electrostatic transducers support above a second plate. When distances are small the transducers can exert very large forces. The momentum carried by approximately

half a wavelength of air molecules is able to set the membrane in motion and vice versa. Electrostatic actuation and detection enables the realization and control of such membranes. Alternatively the membranes can be actuated using piezoelectric and magnetic transducers.

Broad band microfabricated capacitive ultrasonic transducers (cMUTs) may include multiple elements including identical or different size and shape membranes supported above a silicon substrate by walls of an insulating material which together with the membrane and substrate define cells. The walls are formed by micromachining a layer of insulation material such as silicon oxide, silicon nitride, etc. The substrate can be glass or other substrate material. The capacitive transducer is formed by a conductive layer or the membrane and conductive means such as a layer either applied to the substrate or the substrate having conductive regions. In other types of broadband ultrasonic transducers in which the membranes are actuated by piezoelectric transducers (pMUTs) the cell walls need not be made of insulating material.

The fabrication of capacitive micromachined ultrasonic transducers has been described in many publications and patents. For example U.S. Patent Nos. 5,619,476; 5,870,351 and 5,894,452, incorporated herein by reference, describe the fabrication of capacitive or electrostatic type ultrasonic transducers in which the membranes are supported above a substrate such as silicon by insulative supports such as silicon nitride, silicon oxide or polyamide. The supports engage the edges of each membrane to form a cell or cells. A voltage applied between the substrate and conductive film on the surface of the membranes causes the membranes to vibrate and emits sound, or in the alternative, received sound waves cause the membranes to vibrate and provide a change in capacitance. The membranes can be sealed to provide operation of the transducers immersed in liquids. Generally the transducers include a plurality of cells of the same or different sizes and/or shapes. In some applications the multi-cell transducer elements are disposed in arrays with the electrical excitation of the elements controlled to provide desired beam patterns. The same technology can be employed to fabricate pMUTs and mMUTs.

Generally the membranes in the prior art cMUTs are grown or deposited on an insulating film and the insulating film is selectively etched through openings in the membrane to provide underlying cavities. Membrane properties which depend upon the process parameters and the predictability, reproducibility and uniformity of the membranes are compromised. Further the formation of membranes with underlying cavities requires complex processing steps. Furthermore it is difficult to generate complex cavity membrane structures using the conventional MUT fabrication technology of the prior art.

OBJECTS AND SUMMARY OF THE INVENTION

It is a general object of the present invention to provide a method of fabricating micromachined ultrasonic transducers by employing fusion wafer bonding technology.

It is another object of the present invention to provide a method of fabricating MUTs with cells having fusion bonded membranes having prescribed properties.

It is a further object of the present invention to provide MUTs with membranes made of single crystal silicon whose mechanical properties are well known and do not depend on process parameters.

It is another object of the present invention to provide a method of fabricating MUTs in which the membrane is formed from the silicon on a silicon-on-insulator (SOI) wafer.

It is a further object of the present invention to provide a method of fabricating MUTs in which the shape and size of the membrane are defined by photolithography techniques which allows the building of membranes of virtually any size and shape.

It is a further object of the present invention to provide a method of fabricating MUTs with single crystal membranes having regions of different thickness.

There is provided a method of fabricating MUTs which employs photolithographic definition and etching of an oxide layer to define cavity size and shapes of the MUT cells, fusion bonding of the silicon side of a silicon-on-insulator wafer, the oxide layer and a support wafer, removal of the back side and the oxide layer of the silicon-on-insulator wafer to form a silicon membrane and to MUTs which include as a membrane the silicon layer of an SOI wafer.

There is provided a method of fabricating MUTs having cells with membranes supported by a substrate which employs photolithographic definition and etching to form cell walls of selected shape and cavity size, providing a wafer which includes a layer of material which is to form the membrane and fusion bonding the layer to the cell walls and a support substrate, removing the wafer to leave the layer of material to form the membrane whereby to form walls defined by the membrane, cell walls and the substrate.

There is provided a method of fabricating cMUTs comprising selecting a silicon wafer and a silicon-on-insulator wafer, forming a thermal oxide layer of predetermined thickness on the silicon of the wafer or on the silicon of the SOI wafer, defining the shape and size of the cavity by selectively removing the thermal oxide by photolithography and etching, fusion

bonding the wafers and removing the insulator and oxide from the silicon-on-insulator wafer to leave the silicon layer to form a membrane supported on the patterned oxide.

There is provided a capacitive micromachined ultrasonic transducer in which the transducer membrane comprises the silicon layer of a silicon-on-insulator wafer.

BRIEF DESCRIPTION OF THE DRAWINGS

The foregoing and other objects of the invention will be more clearly understood from the following description when read in conjunction with the accompanying drawings of which:

Figures 1.1 through 1.9 illustrates the steps of forming a cMUT in accordance with one embodiment of the present invention;

Figure 2 is a sectional view illustrating an alternative embodiment of the processed wafer of Figure 1.3;

Figures 3.1 through 3.7 illustrates the steps in forming a cMUT in accordance with another embodiment of the present invention;

Figures 4.1 through 4.3 illustrates the steps in forming a cMUT in accordance with still a further embodiment of the present invention;

Figures 5.1 through 5.6 illustrates the steps in forming a cMUT including a membrane having portions of different thicknesses in accordance with still another embodiment of the present invention;

Figure 6 illustrates a cMUT in accordance with a further embodiment of the invention;

Figure 7 illustrates a cMUT in accordance with another embodiment of the present invention;

Figure 8 illustrates the first and second resonant frequencies in air as a function of the extra mass on the membrane of Figure 7;

Figure 9 illustrates the ratio of the first and second resonance frequencies of Figure 8;

Figure 10 illustrates a cMUT in accordance with still another embodiment of the present invention;

Figure 11 illustrates a pMUT fabricated in accordance with another embodiment of the present invention;

Figures 12 and 13 illustrates mMUTs fabricated in accordance with another embodiment of the present invention;

Figure 14 schematically illustrates the formation of a then layer which serves as a membrane for fusion bonding in accordance with the present invention; and

Figures 15.1 – 15.4 illustrates the steps of forming another membrane for fusion bonding in accordance with the present invention.

DESCRIPTION OF PREFERRED EMBODIMENT(S)

The fabrication of cMUTs having silicon membranes formed by fusion bonding of silicon-on-oxide wafers to silicon oxide cell wall is first described followed by a description of use of the same technology to form pMUTs and mMUTs. This is followed by a description of using the same fusion bonding process to fabricate other types of membranes having selected characteristics.

Referring to Figures 1.9 and 3.6, cMUTs in accordance with the present invention include cells on a support wafer 11 with a plurality of cells 12 having oxide walls 13 and silicon membranes 14 formed by fusion bonding of the silicon of a silicon-on-oxide wafer to the oxide walls. Conductive electrodes comprise the wafer 11 and the conduction layers 16 (Figure 1.9). In Figure 3.7 where like parts are represented by the same reference numbers the electrodes comprise the implanted region 17 and the conductive layers 16.

The steps of forming cMUTs in accordance with Figure 1.9 employ fusion wafer bonding under vacuum are illustrated and described with reference to Figures 1.1 through 1.9. The process starts with two wafers. The first wafer 11 is a prime quality silicon wafer which is called a carrier wafer (Figure 1.1). This wafer will make up the bottom electrode of the cMUTs. It can be a low resistivity wafer which makes it a conductive backplate or it can be a high resistivity wafer and doped selectively to define a patterned back electrode. The second wafer is a silicon-on-insulator (SOI) wafer as illustrated in Figure 1.5. The silicon thickness of the SOI wafer will determine the membrane thickness. The SOI wafer includes a silicon support wafer 21, an oxide layer 22 and the silicon layer 14 which forms the cMUT membranes. The SOI wafer is chosen to meet the design requirements for thickness and characteristics of the membrane.

The first steps are to define cavity size and shape. First the carrier wafer is thermally oxidized to form oxide layers 24 and 26 (Figure 1.2). The thermal oxide thickness determines the cavity height of the cMUT. It is chosen to meet the design requirements. A photolithography step forms a suitable mask with openings defining the cavity shape. This is followed by an etch step such as a plasma etch to define the cavity. It is apparent that the

cavities can be of virtually any size and shape (Figure 1.3). The dry etching of the silicon dioxide layer stops at the silicon wafer so that the cavity depth is determined by the initial thermal of oxide. If it is desired to have deeper cavities, an additional silicon etch (dry or wet) can be used to define a deeper cavity if needed as illustrated in Figure 2. In order to establish an electrical isolation between the bottom electrode and the top electrode (the SOI silicon) a thin layer of oxide 27 is thermally grown on the carrier wafer as shown in Figure 1.4. This prevents possible shorts and device failure if the membrane is collapsed to a point where it contacts the bottom of the cavity.

The next step is to form the cMUT membrane. The SOI wafer is placed over the carrier wafer with the thin silicon layer 14 facing the carrier wafer, Figure 1.6. The two wafers are then bonded by fusion wafer bonding under vacuum. If the bonding is done under very low pressure, the formed cavities or cells are vacuum sealed. Following this step the thick silicon portion 21 of the SOI support wafer on the back side and the oxide layer 22 are removed, Figure 1.7. This can be done by a grinding and etching process whereby only the thin silicon layer which forms the membrane over the cavities remains, Figure 1.7. The oxide layer 26 on the carrier wafer is also removed. The next step is to form the top electrodes. However, prior to the electrode formation another photolithography and dry etch sequence can be performed. With this step the top silicon and oxide layers around the periphery of the device are removed as shown in Figure 1.8. There are two reasons for this, one is to isolate individual elements electrically from neighboring elements in an array. The other reason is to make electrical contact to the carrier wafer which makes up the bottom electrode of the cMUT. A thin layer of metal 16 is then deposited over the membrane to make up the top electrode, Figure 1.9. The top electrode can be patterned by photolithography and etch sequences to reduce parasitic capacitance. Thus there are formed cMUTs having evacuated cells or cavities with a single crystal silicon membrane whose thickness and characteristics can be controlled by controlling the fabrication of the SOI wafer.

Using the fusion wafer bonding techniques and SOI wafers, cMUTs with electrical through wafer interconnects can be fabricated. In this embodiment the carrier wafer is processed to provide through wafer interconnects. A wafer with through wafer interconnect is illustrated in Figure 3.4. The wafer is preprocessed with the electrical through wafer interconnect technology so that the electrical connections, both signal and ground, of the front side pads have connections on the back side of the carrier wafer. Briefly, the interconnect wafer includes a body of high resistivity silicon 31 into which have been implanted N type and P type regions forming a pn

junction 32, a thermal oxide layer 33 is grown for isolation. The wafer with through wafer interconnects could be processed in the same manner as the wafer of Figure 1.1 to define the cavities having silicon oxide walls onto which is fusion bonded the SOI wafer. However, a totally different process can be practiced for forming the device shown in Figure 3.6. The SOI wafer of Figure 3.1 including a back support 21, oxide layer 22 and silicon layer is thermally oxidized, Figure 3.2, with the resulting silicon oxide layer 34 with thickness which determines cavity depth. The initial SOI wafer and the thermal oxidation conditions are chosen to meet the design requirements for membrane thickness and characteristics and cavity depth. A photolithography and dry etch sequence follows the thermal oxidation step to define the cavity shape and size which is equivalent to the membrane shape and size, Figure 3.7. The formation of membrane is very similar to the one described above. The SOI wafer and carrier wafer are fusion bonded, Figure 3.4, using fusion bonding techniques under low pressure resulting in vacuum sealed cavities. The back of the SOI wafer is ground and etched away to remove the silicon and silicon dioxide layers 21, 22 leaving a thin layer of silicon which forms the membrane of the capacitive micromachined ultrasonic transducer. This is followed by a metallization step which is slightly different from the one described above. In this case the top electrode serves as the ground and is therefore connected to the silicon substrate of the carrier as shown at 34 in Figure 3.7. In the case of two-dimensional cMUT arrays for which the electrical through wafer interconnect are most relevant the top electrode is the ground electrodes and connects all the array elements. On the other hand, the signal electrode of each element is individually brought back to the back side of the carrier wafer through the electrical through wafer interconnects. It is apparent from the foregoing two processes that the size and configuration is determined by photolithographic steps the cavity depth by oxide thickness and etching, and the membrane characteristics by the thin silicon layer of the SOI wafer. In all instances the cavities are vacuum sealed and the cMUT is operable both in air and in submersion applications.

The wafer bonding technology for fabricating cMUTs allows the design of complex cavities. In this way it is possible to solve some of the problems associated with cMUTs. The following is one variation of the wafer bonding technology to create a complex cavity structure with non-bonded posts which may be used in various applications. For example it may be used to solve the big deflection and stiffening problem due to large initial pressure loads for cMUT applications in the low frequency range. Referring to Figure 4.1, the starting materials are the

same as used in connection with the embodiment of Figures 1.1 through 1.9. The first part of the cavity definition is identical to the one described with regard to Figure 1.3 (Figure 4.1). Another photolithography a dry silicon etch step is used to define a second cavity structure inside of the first cavity as shown in Figure 4.2. A short thermal oxidation step follows to create a thin layer of oxide 42 on the silicon to establish an electrical isolation between the bottom and top electrodes. Membrane formation and electrode definition is identical to that described with regard to Figures 1.5 through 1.9 and results in the device of Figure 4.3 which shows supporting oxide posts 43 and non-bonded post 44.

As is apparent from the foregoing, in cMUT transducers the membranes are supported from their edges. That is, the edges of the membranes are clamped and therefore do not move. As one goes toward the center of the membrane, the movement in response to actuation voltages increases. In other words the edges of the membrane do not contribute to the radiated pressure as much as the center which actually means a loss of efficiency. Using the flexibility of the wafer bond technology, cMUTs can be designed with piston-like movements which results in increased efficiency. This is achieved by putting an extra mass at the center of the membrane. Moreover, in a usual cMUT membrane thickness is uniform through the membrane, which determines both the spring constant and the mass. There are two critical parameters that determine the mechanical response of the cMUT. By using wafer bond technology to fabricate cMUTs, one can put extra mass at the center of the membrane and adjust the spring constant and the mass of the membrane independently. For a fixed design frequency one can select different effective mass and spring constants selection of the location of the piston part one can manipulate the harmonic response of the cMUT. The process flow illustrated in Figures 5.1 through 5.7 illustrate methods of fabricating cMUTs with piston-like membranes.

In fabricating a device one starts with two SOI wafers and a prime quality silicon wafers. The first step is to define the extra mass. For this purpose the first SOI wafer is patterned with a photolithographic and dry etch sequence which defines the extra mass areas which will stick to the membrane, Figure 5.1. In this step the thin silicon layer of the SOI wafer is selectively etched to leave regions or islands of predetermined shape, size and thickness to meet the design requirements for the added mass to be introduced to the membrane. This wafer is then fusion bonded to the second SOI wafer as illustrated in Figure 5.2. The support portion, an oxide of the first SOI wafer, is ground and etched away, leaving leaving an SOI wafer with extra mass of silicon 51 on the silicon layer 52 of the second SOI wafer.

The prime quality carrier silicon wafer 11 is thermally oxidized to define the cavity depth and the cavity shape and size are defined photolithographically and dry etch sequence removes the exposed oxide. The cavity depth must be larger than the thickness of the extra mass on the thin silicon layer of the SOI wafer. Depending on the design, thermal oxidation may not be enough to define the cavity depth, and a further silicon etch may be required as illustrated in Figure 2. The carrier wafer is then thermally oxidized 57 again to grow the thin layer of silicon dioxide for electrical isolation purposes, Figure 5.4. The carrier wafer and the SOI wafer with the extra silicon mass on the thin silicon layer are fuse bonded under vacuum as illustrated in Figure 5.5. The extra masses on the SOI wafer are aligned with the cavities on the carrier wafer. The handle portion or the support portion of the SOI wafer together with the silicon dioxide is removed by grinding and etching, leaving the silicon membrane with extra silicon masses and vacuum sealed cavities such as shown in Figure 5.6 which also shows the application of electrodes by following the steps of isolation and electrode definition described in relation to Figures 1.8 and 1.9. The cMUT includes membrane 14 with extra mass 51, cavities 12, and electrodes 16. Alternatively, the oxide can be formed on the silicon of the SOI wafer as in the process of Figure 3.

By combining complex cavity structures such as those described with regard to Figure 4 and membranes with extra masses as described in relation to Figure 5, one can achieve all the advantages of both. Such a device is illustrated in Figure 6 where like reference numbers are applied to like parts.

cMUTs are resonant structures in air with a fairly high quality factor. However, in immersion the acoustic impedance of the medium dominates the mechanical impedance of the cMUT, resulting in a very broad band operating frequency. Over 100% bandwidth are typical with cMUTs. It is possible to increase the bandwidth of the cMUTs further by using an extra mass underneath the membrane which is made possible with the foregoing described wafer bonding technology. In immersion the lower end of the frequency response of the cMUT is determined by the overall size of the transducer. When the frequency becomes so low the device is much smaller than a wavelength, the output pressure of the cMUT drops. The higher end of the cMUT's frequency response is limited by the second resonance of the membranes. By pushing the second resonance of the cMUT membranes at the higher frequencies it is possible to increase the bandwidth. For example an extra mass defined in the shape of a ring 61 formed on the membrane 62 supported on the carrier wafer 63 by oxide layer 64. The dimensions are

shown in Figure 7 for one example. Figure 8 shows a plot of the first two resonant frequencies of the membrane shown in Figure 7 as a function of thickness of the mass. Figure 9 is a plot of the ratio of the two frequencies showing a definite increase in second resonance frequency with respect to the first.

The method of creating complex cavity structures described with regard to Figure 4 can be used to address other problems. Instead of posts inside the cavity, pistons can be created as shown in Figure 10. One of the problems this structure can bring solution to is the parasitic capacitance. In a cMUT any non-moving capacitance, and any fringing capacitance is considered as a parasitic capacitance because they neither generate or detect any acoustic waves. Normally the top electrode is patterned to reduce the parasitic capacitance by minimizing the metallization area over the non-moving region. The bottom electrode can be patterned too, to decrease the parasitic capacitance further. But still there will be unavoidable fringing capacitance. Using the wafer bonding technology to make cMUTs, one can design and master the cavity shape to minimize fringing fields which would further improve the performance of a cMUT.

As briefly described above, the same fusion bonding process can be employed to fabricate pMUTs and mMUTs. Rather than applying a conductive layer to form cMUTs, Figures 1.9, 4.3, 5.6, 6 and 7, one may form a piezoelectric transducer or a magnetic transducer on the membrane. This is schematically illustrated in Figures 11, 12 and 13 for a single cell.

Referring to Figure 11, the cell includes a substrate 51 which is micromachined to form cell walls 52. The cell walls can also be formed by micromachining oxide or other layers. The membrane 53 is fusion bonded to the walls and piezoelectric transducer 54 is deposited onto the membrane. The transdcuer includes metal electrodes 56, 57 and piezoelectric material 58. A voltage applied between the electrodes generates stress in the piezoelectric material and vibrates the membrane to generate acoustic waves. Stress in the piezoelectric material is measured acoustic waves received by the pMUT.

In Figures 12 and 13 like reference numerals have been applied to parts like those of Figure 11. Figure 12 shows a coil 61 on the membrane 53 while Figure 13 shows a magnetic material 62 on the membrane 53. The membrane is vibrated by magnetic fields 63 to generate acoustic waves or vibration of the membrane is magnetically sensed.

Although silicon membranes fabricated by fusion bonding silicon-on-oxide wafers to form cells has been described, the fusion bonding of membranes of other materials can be

implemented. For example the membrane may be formed by depositing or epitaxially growing a film of material 66 (e.g. Si_x, N_x, Sil, etc.) onto a carrier wafer 67 of sacrificial material, Figure 14, which can be removed after the film or layer has been fusion bonded to form the cell membrane. In the alternative the membrane can be defined by fusion bonding a wafer of desired material and then removing wafer material by etching, grinding and polishing to leave a membrane of desired thickness.

In a further method a wafer 68, Figure 15.1, of the desired membrane material is implanted to form a highly stressed interface 69 and fusion bonded to the walls 71 of cells 72, Figure 15.2. The assembly is then subjected to a thermal cycle (shock) to separate the thin layer of stressed material from the bulk, Figure 15.3, and then fine polished, Figure 15.4, leaving MUTs with a membrane 73 of selected material and characteristics.

Thus there have been provided MUTs having a membrane whose thickness and characteristics can be closely controlled to provide increased predictability, uniformity and repeatability of MUT devices. Furthermore, MUT devices can be configured to provide enhanced operation such as improved acoustic characteristics and reduction of parasitic capacitance.

CLAIMS

What is claimed is:

1. The method of fabricating a microfabricated ultrasonic transducer comprising the steps of:

selecting a silicon carrier wafer;

selecting a silicon-on-insulator wafer having a thin silicon layer supported on an oxide layer;

thermally oxidizing either the silicon wafer or the silicon layer of the silicon-on-insulator wafer to form a silicon oxide layer of predetermined thickness;

applying a mask having openings of predetermined size and shape, to expose areas of the oxide layer;

etching away the oxide at the exposed openings to define oxide walls;

bonding the two wafers with the thin silicon layer facing the silicon carrier wafer and spaced therefrom by the oxide layer whereby cells are formed; and

removing the wafer and oxide layer of the silicon-on-oxide-on insulator wafer leaving the thin silicon membrane supported spaced from the silicon carrier wafer by the silicon oxide.

2. A method as in claim 1 in which the oxide layer is formed on the silicon carrier wafer.

3. The method of claim 1 in which the oxide is formed on the silicon layer of the silicon-on-oxide insulator.

4. The method as in claim 2 including the additional step of applying a thin oxide layer over the support oxide and carrier wafer prior to bonding.

5. The method of claim 3 including the steps of forming a thin oxide layer on the carrier wafer prior to bonding the wafers.

6. The method of claim 1 including the additional steps of selecting an additional silicon-on-insulator wafer having a thin silicon layer supported on an oxide layer;

masking an etching away portions of said thin silicon layer to leave islands of predetermined size and shape;

bonding said islands to the thin silicon of the silicon-on-insulator wafer;

removing the oxide and wafer to leave the selected wafer with a thin silicon layer having areas of different thicknesses whereby the resulting silicon membranes have areas of different thicknesses.

7. The method of claim 2 including the additional step of etching the carrier wafer between the oxide cavity walls to configure the bottom wall.

8. The method of claim 3 including the additional step of etching the carrier wafer between the oxide cavity walls to configure the bottom wall.

9. The method of forming an ultrasonic transducer the type comprising a membrane supported on a carrier wafer by patterened oxide supports of predetermined size and shape;

selecting a carrier wafer;

selecting a silicon-on-insulator wafer having a thin silicon layer supported by an oxide;

forming an oxide layer of predetermined thickness and by masking and etching removing the oxide layer from selected regions to provide regions of predetermined size and shape;

bonding the carrier and silicon of the silicon-on-insulator wafer; and

removing the support oxide and wafer leaving the silicon layer to form membranes which defines cavities of predetermined size and shape.

10. An ultrasonic transducer the type having cells with one wall defined by membrane comprising:

a silicon body having a surface forming one wall of the cavity;

a silicon oxide layer configured to define the side walls of said cavities; and

a membrane supported fused to and supported space from the silicon body by said silicon oxide walls to define with said silicon body and said cells.

11. An ultrasonic transducer as in claim 10 wherein said silicon membrane at each of said cells has regions of different thickness.

12. An ultrasonic transducer as in claim 10 wherein said silicon body is configured with regions of different height at each of said cells.

13. An ultrasonic transducer as in claim 10 wherein said silicon membrane at each of said cell has regions of different thicknesses and wherein said silicon body is configured with regions of different height at each of said cavities.

14. An ultrasonic transducer as in claim 10 wherein the single crystal membrane is formed by the silicon layer of a silicon-on-insulator wafer.

15. The method of fabricating a micromachined ultrasonic transducer which comprises the steps of:

micromachining a carrier wafer to form cavities of selected size and shape, said cavities having membrane support walls; and

fusion bonding a membrane of selected material having selected mechanical characteristics to said support walls whereby to form cells.

16. The method of claim 15 which includes the step of forming a piezoelectric transducer on the membrane of each of said cells.

17. The method of claim 15 which includes the step of forming a magnetic transducer on the membrane of each of said cells.

18. The method of claim 15 which includes the step of forming a conductor electrode on said membrane whereby it can be electrostatically vibrated.

19. The method of claim 15 in which the membrane is a layer supported on sacrificial material and the sacrificial material is removed after the fusion bonding.

20. The method of claim 15 in which the layer is a stressed region in a sacrificial material and the unstressed material is removed by thermal shock.

21. The method of fabricating ultrasonic transducers which comprises the steps of defining cavities by micromachining a support structure and fusion bonding under vacuum a membrane to the support structure to seal the cavities and form evacuated cells.

22. The method of claim 21 including the steps of forming piezoelectric transducer to vibrate the membrane.

23. The method of claim 21 including the steps of forming magnetic transducer to vibrate the membrane.

24. The method of claim 21 including the steps of forming electrostatic transducers to vibrate the membrane.

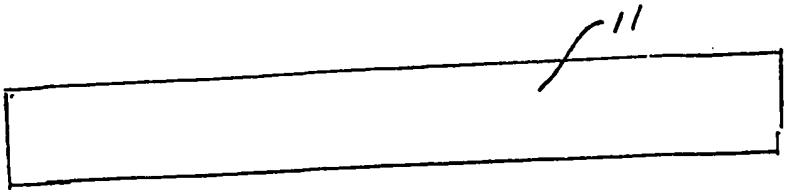


Figure 1.1

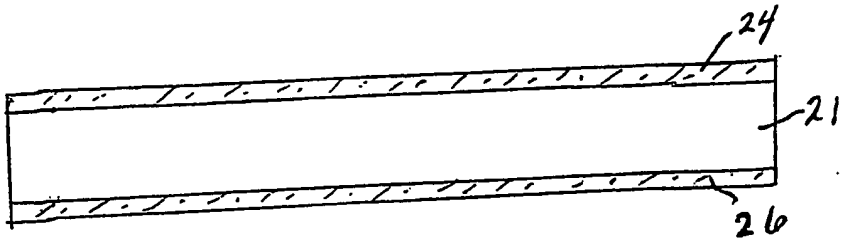


Figure 1.2

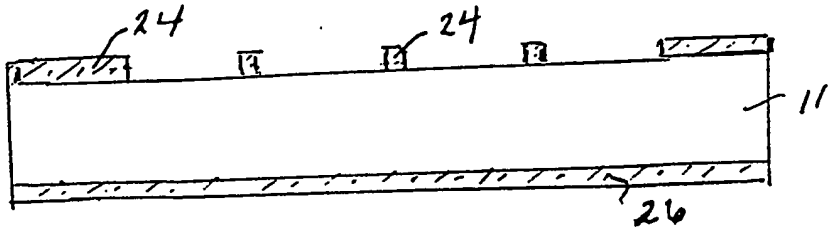


Figure 1.3

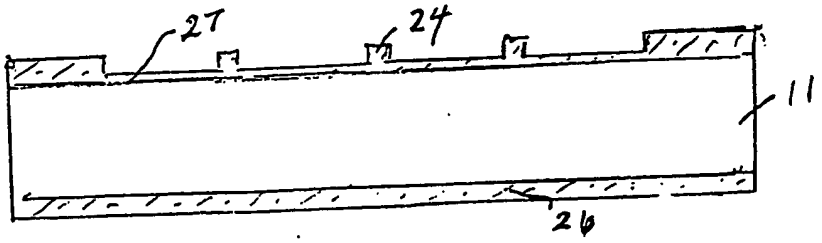


Figure 1.4

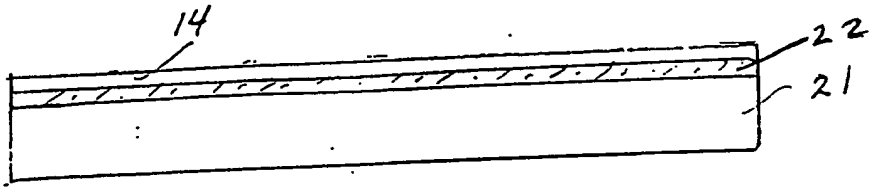


Figure 1.5

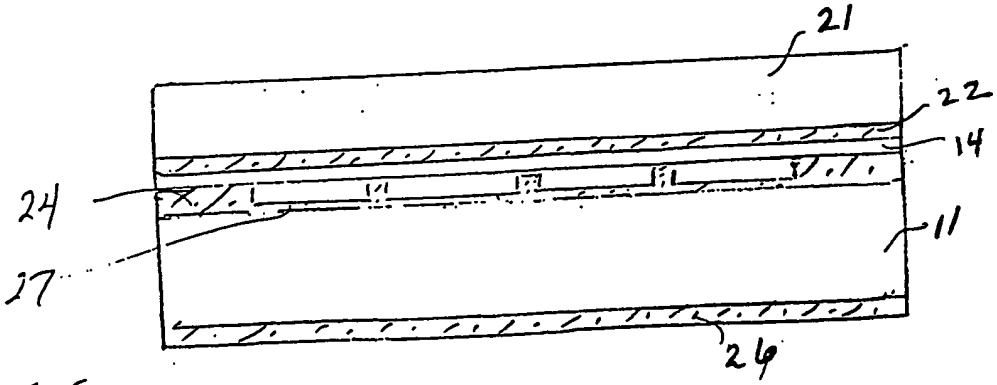


Figure 1.6

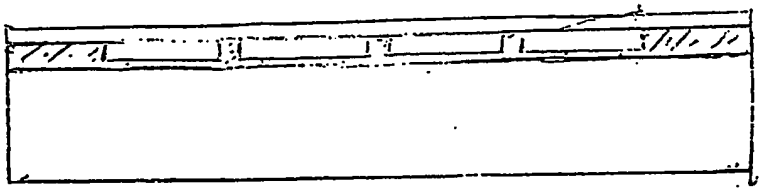


Figure 1.7

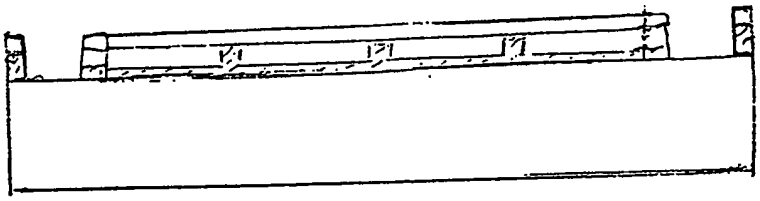


Figure 1.8

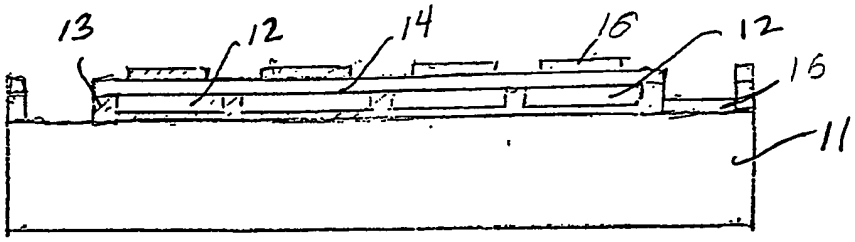


Figure 1.9

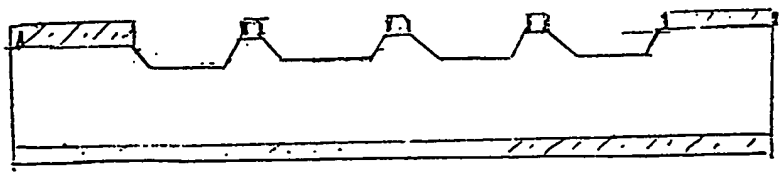


Figure 2

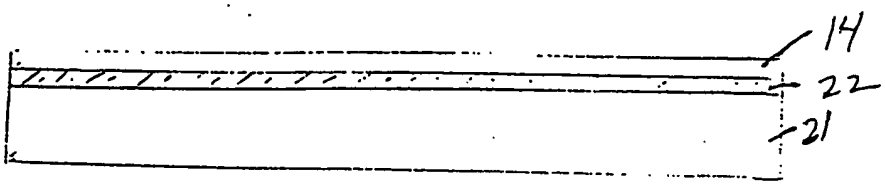


Figure 3.1

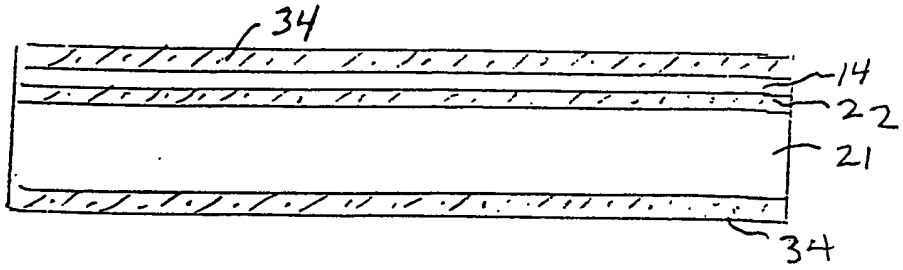


Figure 3.2

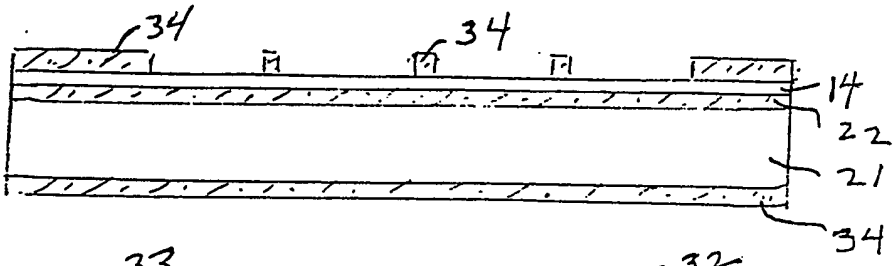


Figure 3.3

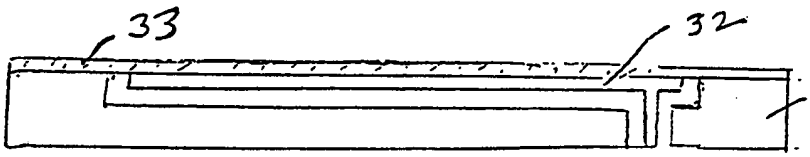


Figure 3.4

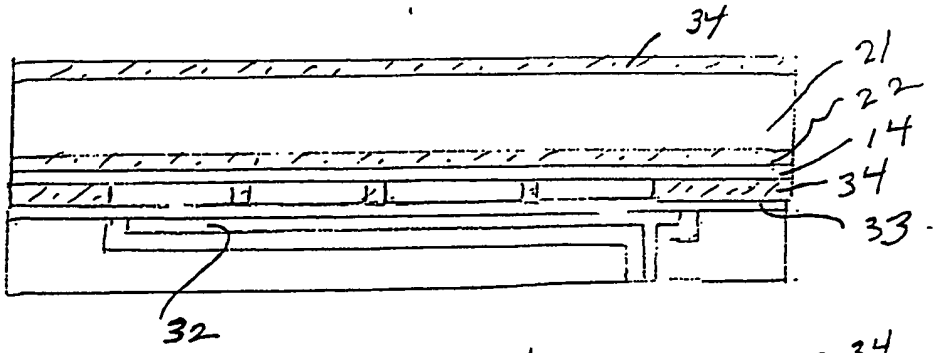


Figure 3.5

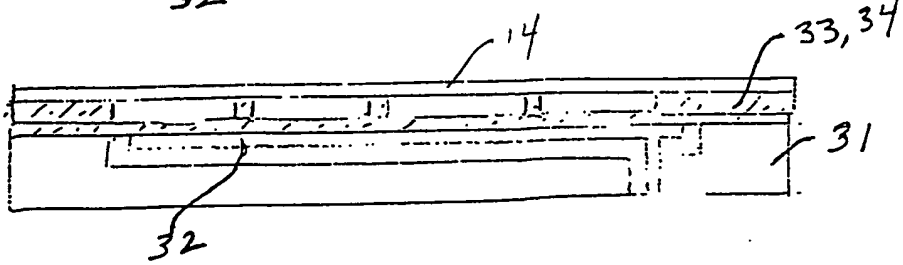


Figure 3.6

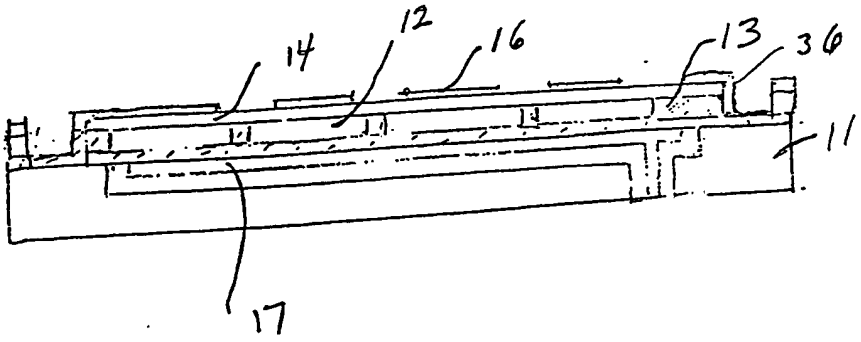


Figure 3.7

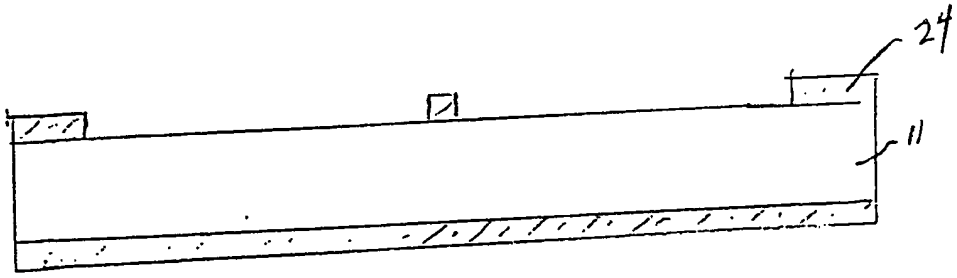


Figure 4.1

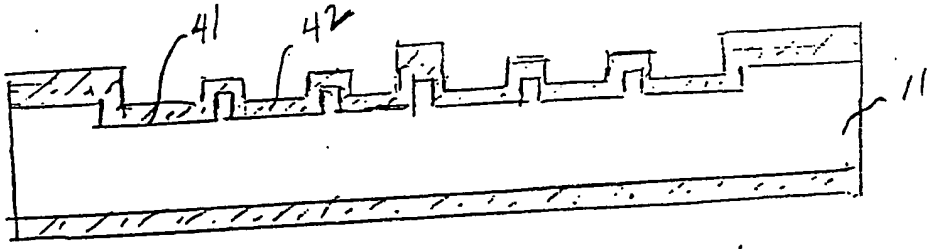


Figure 4.2

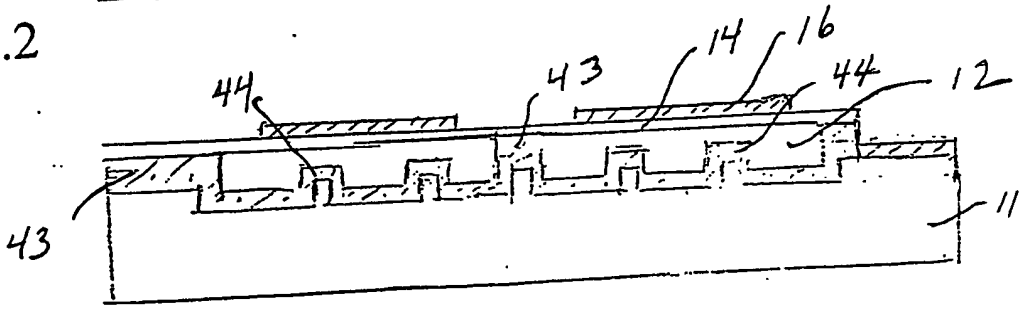


Figure 4.3

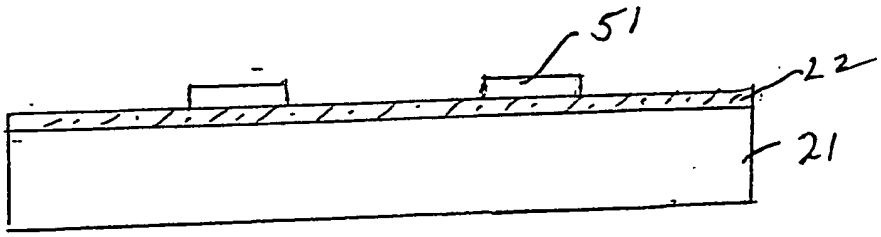


Figure 5.1

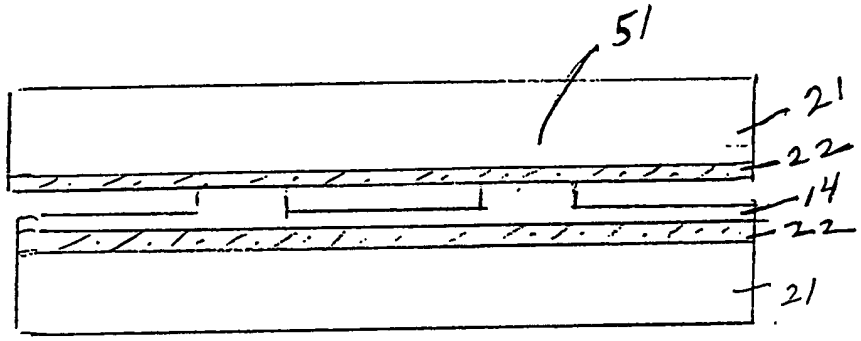


Figure 5.2

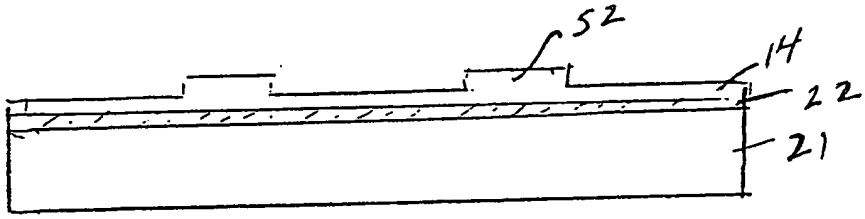


Figure 5.3

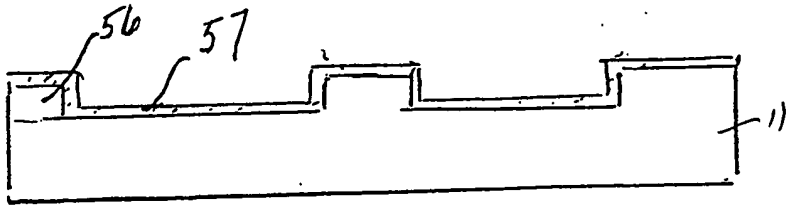


Figure 5.4

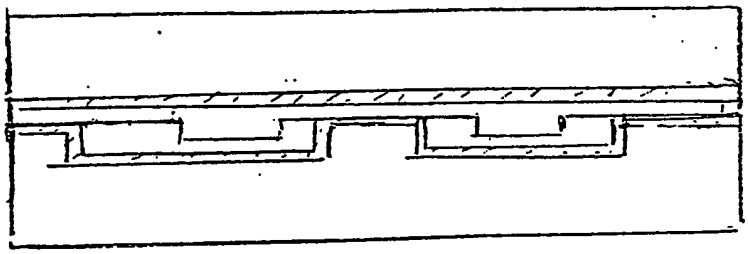


Figure 5.5

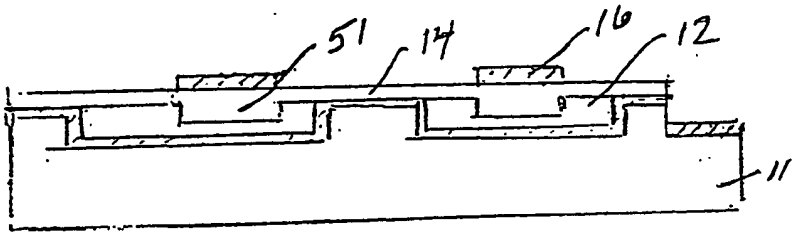


Figure 5.6

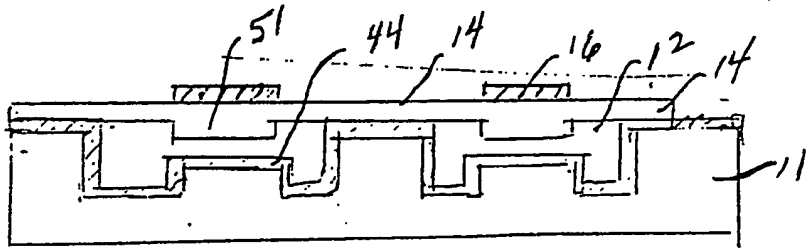


Figure 6

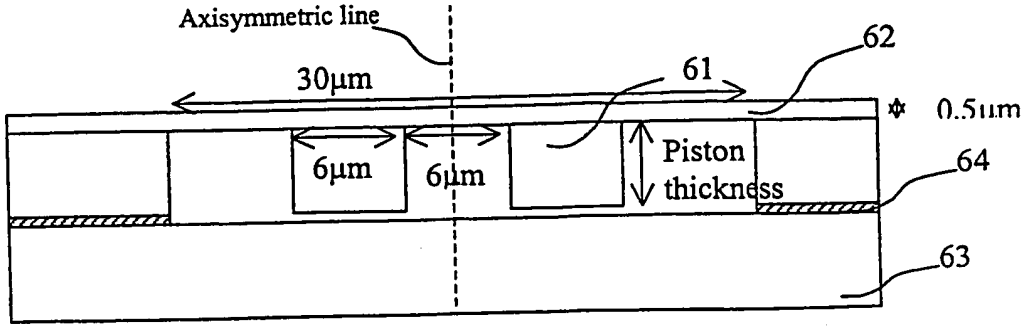


Figure 7

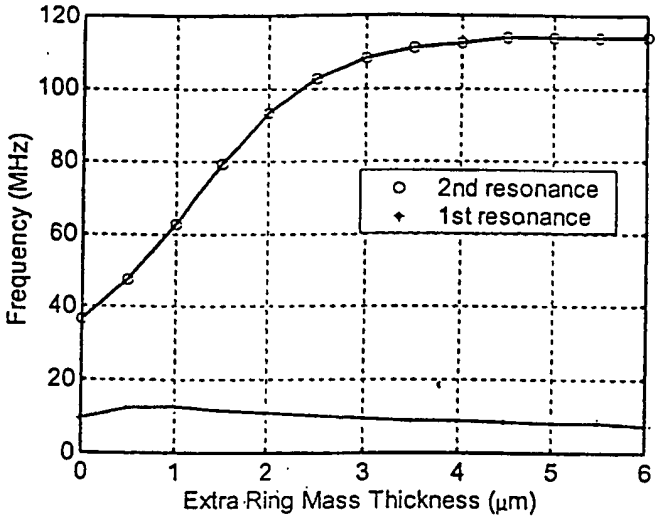


Figure 8

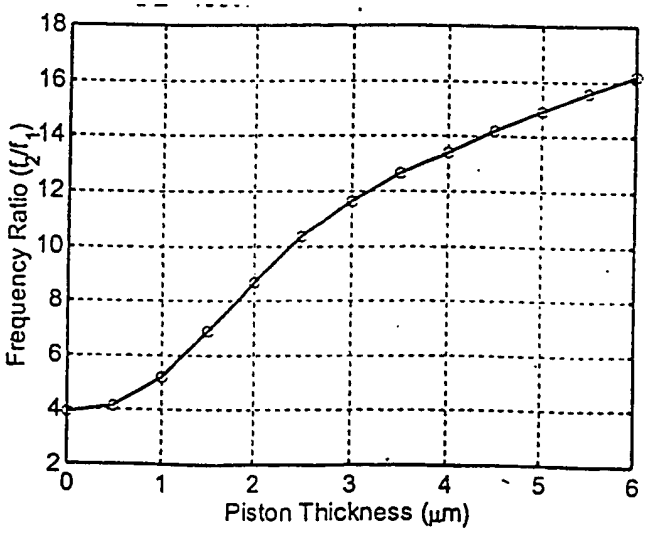


Figure 9

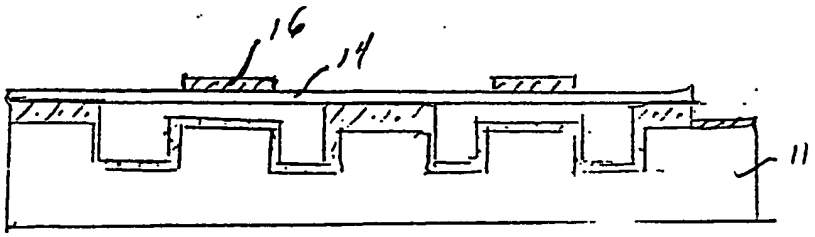


Figure 10

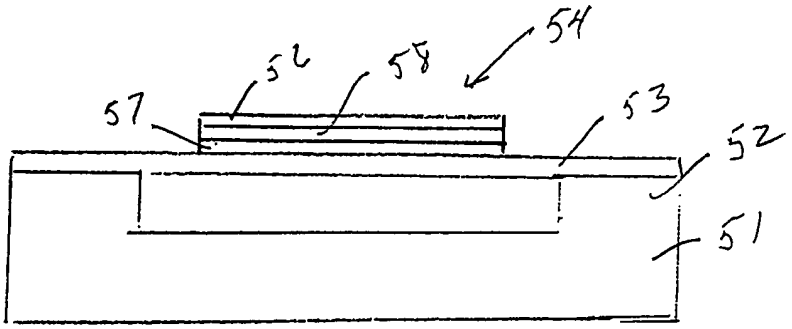


Figure 11

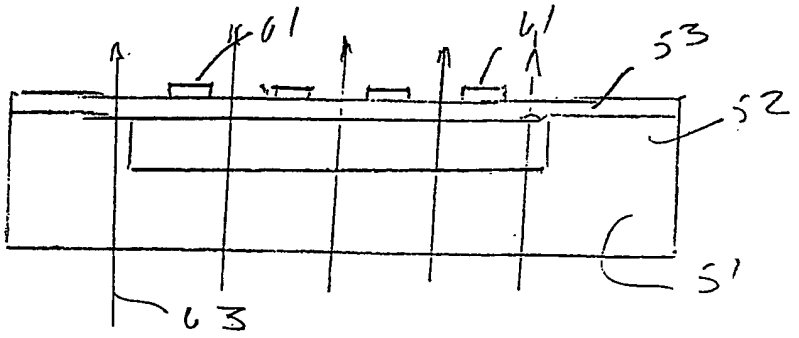


Figure 12

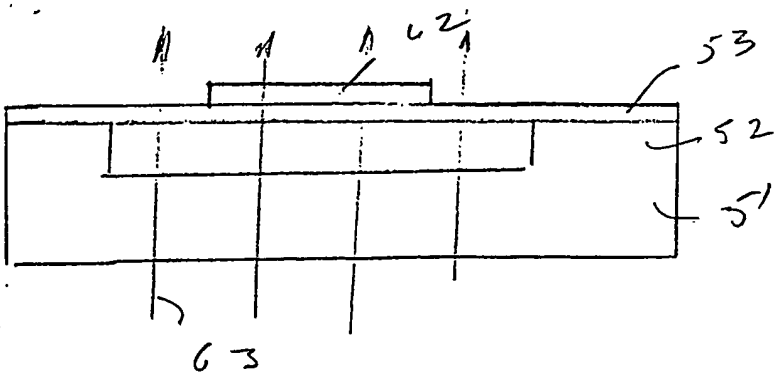


Figure 13

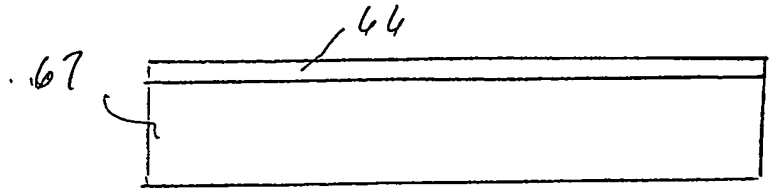


Figure 14

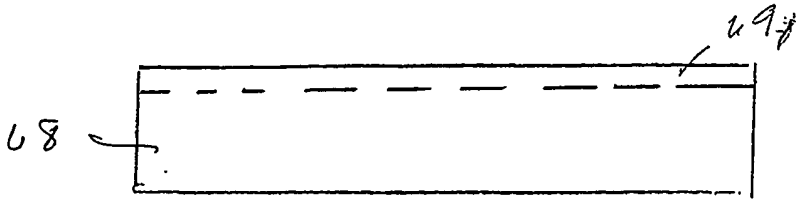


Figure 15.1

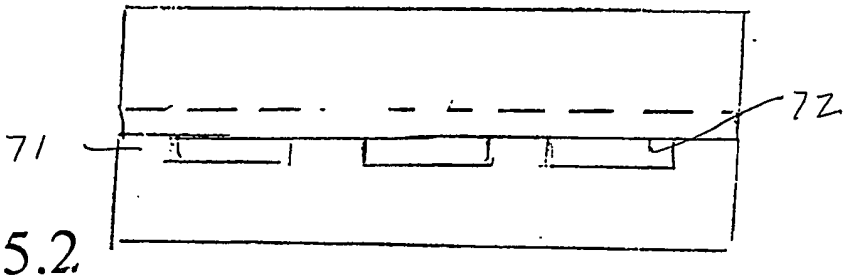


Figure 15.2

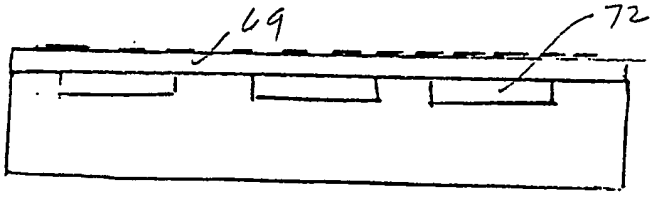


Figure 15.3

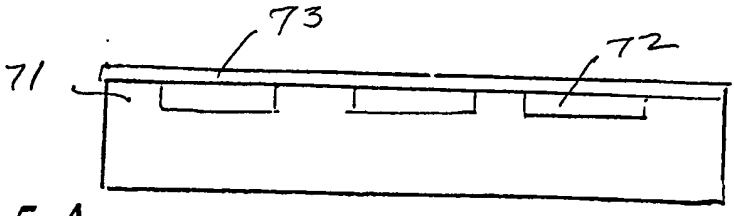


Figure 15.4

(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
19 February 2004 (19.02.2004)

PCT

(10) International Publication Number
WO 2004/016036 A3

(51) International Patent Classification[7]: H04R 19/00

(21) International Application Number: PCT/US2003/024777

(22) International Filing Date: 8 August 2003 (08.08.2003)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
60/402,220 8 August 2002 (08.08.2002) US
10/638,057 7 August 2003 (07.08.2003) US

(71) Applicant *(for all designated States except US)*: **THE BOARD OF TRUSTEES OF THE LELAND STANFORD JUNIOR UNIVERSITY** [US/US]; 1705 El Camino Real, Palo Alto, CA 94306-1106 (US).

(72) Inventors; and

(75) Inventors/Applicants *(for US only)*: **KHURI-YAKUB, Butrus, T.** [US/US]; c/o Stanford University, 1705 Camino Real, Palo Alto, CA 94306-1106 (US). **HUANG, Yongli** [—/US]; c/o Stanford University, 1705 El Camino Real, Palo Alto, CA 94306-1106 (US). **ERGUN, Arif, S.** [TR/US]; c/o Stanford University, 1705 El Camino Real, Palo Alto, CA 94306-1106 (US).

(74) Agents: **TEST, Aldo, J.** et al.; Dorsey & Whitney LLP, 4 Embarcadero Center, Suite 3400, San Francisco, CA 94111 (US).

(81) Designated States *(national)*: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, YU, ZA, ZM, ZW.

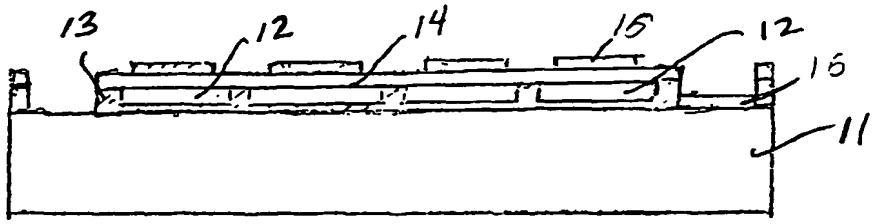
(84) Designated States *(regional)*: ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IT, LU, MC, NL, PT, RO, SE, SI, SK, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:
— *with international search report*
— *before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments*

(88) Date of publication of the international search report: 13 May 2004

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(54) Title: MICROMACHINED ULTRASONIC TRANSDUCERS AND METHOD OF FABRICATION



(57) Abstract: There is described a micromachined ultrasonic transducers (MUTS) and a method of fabrication. The membranes of the transducers are fusion bonded to cavities to form cells. The membranes are formed on a wafer (11) of sacrificial material. This permits handling for fusions bonding. The sacrificial material is then removed to leave the membrane (14). Membranes of silicon, silicon nitride, etc. can be formed on the sacrificial material. Also described are cMUTs, pMUTs and mMUTs.

WO 2004/016036 A3

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US03/24777

A. CLASSIFICATION OF SUBJECT MATTER
IPC(7) : H04R 19/00
US CL : 367/181, 174, 163
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
U.S. : 367/181, 174, 163

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 6,430,109 B1 (KHURI-YAKUB ET AL.) 06 AUGUST 2002 (06.08.2002), see entire document.	1-24
A	EP 03-72583 A2 (HITACHI CORP) 13 JUNE 1990 (13.06.1990), see entire document.	1-24
A	LADABAUM ET AL., THE MICROFABRICATION OF CAPACITIVE ULTRASONIC TRANSDUCERS, IEEE JOURNAL OF MICROELECTROMECHANICAL SYSTEMS, VOL. 7, NO. 3, 03 SEPTEMBER 1998, PAGES 295-301.	

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search
17 March 2004 (17.03.2004)

Date of mailing of the international search report
02 APR 2004

Name and mailing address of the ISA/US
Mail Stop PCT, Attn: ISA/US
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
Facsimile No. (703) 305-3230

Authorized officer
for Daniel Pihulic

Telephone No. 703-308-1113

Form PCT/ISA/210 (second sheet) (July 1998)